Application No. 10/701,491
Amendment dated June 22, 2006
Office Action mail date: February 23, 2006

REMARKS/ARGUMENTS

Claims 1-59 are pending in the application.

Claim 15 stands rejected under 35 U.S.C. § 112 for insufficient antecedent basis. Applicant has amended claim 15, and also claim 50.

Claims 1-3, 5, 15-17, 19, 43-47, 49-52, and 54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nguyen et al. (US 6,972,625) in view of Briskin (US 6,721,117). Claims 29-31, 33, 55-57, and 59 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Goh et al. (US 6,519,106) in view of Briskin and further in view of Nguyen. Applicant respectfully traverses these prior art rejections, and requests reconsideration and allowance of the claims in view of the following arguments.

Applicant appreciates the Examiner's indication of allowability of claims 4, 6-14, 18, 20-28, 32, 34-42, 48, 53, and 58, but decline the Examiner's invitation at this time to rewrite these claims in independent form including all of the limitations of the base claim and any intervening claims, based on the following traversal of the prior art rejection.

In order for the prior art properly to render a claimed invention obvious under 35 U.S.C. § 103(a), the prior art must teach or suggest all of the claimed limitations. As Applicant will discuss below, the prior art lacks teaching or suggestion of correction of an asymmetric signal, and so cannot teach or suggest the claimed invention.

1. The Combination of Nguyen and Briskin Fails to Teach or Suggest Correcting an Asymmetric Signal

The Examiner has agreed that Nguyen fails to teach a number of limitations of claim 1. However, the Examiner has asserted that Briskin supplies the deficiencies of Nguyen, and has

combined Nguyen and Briskin to reject claim 1. Applicant respectfully disagrees because, while claim 1 recites a circuit for correcting an asymmetric signal, neither Nguyen nor Briskin is related to correcting an asymmetric signal; there is no suggestion or motivation to combine Nguyen and Briskin; and because both references fail to teach or suggest the correction of an asymmetric signal, their combination must be similarly deficient.

Nguyen's purpose is to provide amplifiers with an increased dynamic range in designing receivers to decrease distortion and to relax systems requirements (Nguyen, col. 2, lines 13-15). The Examiner has asserted that Nguyen teaches a variable gain amplifier circuit, referring to Figs. 74-77 of Nguyen. However, the variable gain amplifier circuit in Nguyen maintains *a linear gain* for input verses output signals (Nguyen, col. 98, lines 65-67). Nguyen states:

> In a linear gain, *a 1 dB increase in sinusoidal input signal level produces a 1 dB change in the output signal level at that same frequency.* A gain of this nature is termed a "linear response." If a 1 dB change is not produced, this is indicative of an available power being diverted to produce a signal at another frequency of operation. A signal at a frequency other than desired often interferes with the signal being amplified and is termed distortion. Thus, the linearity of an amplifier is a figure of merit, the greater the linearity the better the quality of the amplifier. (Nguyen, col. 99, lines 4-13, emphasis added).

Nguyen also states:

> A set of three control signals 7404 are supplied to the VGA 3403 from a linearization circuit 7402. The linearization circuit 7402 produces the three control signals 7404 that are derived from a single control signal, V_c 7406 through compensation circuitry. Control signal V_c tends to be proportional to the gain desired in the VGA 3403. *The three control signals 7404 control the VGA in a manner such that a desired gain and a desired linearity tend to be produced by the VGA.*

(Nguyen, col. 99, lines 35-43, emphasis added).

Thus, the VGA circuit in Nguyen referred to by the Examiner maintains a linear gain for input signals. It has nothing whatsoever to do with correcting an asymmetric signal. In fact, Nguyen tries to keep the waveform of the output signal the same as that of the input signal. Thus, Nguyen actually teaches away from correcting an asymmetric signal.

Briskin's purpose is to provide a read/write system that compensates both *input voltage offset and input current offset to reduce write-to-read transition recovery time*, while increasing input impedance to reduce the size of the input capacitors (Briskin, col. 2, lines 26-30). Briskin is irrelevant to correcting an asymmetric signal.

Nguyen and Briskin have completely different purposes and solve completely different problems. There is no reason for a skilled artisan to combine them. Moreover, neither reference relates to a circuit for correcting an asymmetric signal, so that even if a combination of these references were appropriate, the combination would not yield the claimed invention.

Claim 1 recites a g_m switch coupled to the first output of a variable gain amplifier circuit. The Examiner has agreed that Nguyen failed to teach a g_m switch. However, the Examiner has asserted that Briskin teaches a g_m stage, and that the motivation to add the g_m stage in Briskin to the VGA circuit in Nguyen is to provide the Nguyen circuit "the ability to selectively switch input voltage offset compensation between positive and negative shunt feedback, thus suppressing disturbance". However, as discussed above, the VGA circuit in Nguyen is used to produce a signal that is a reproduction of an input signal at an amplified level with a linear gain. The Nguyen circuit does not need the ability to selectively switch input voltage offset compensation between positive and negative shunt feedback.

Further, the Examiner has agreed that Nguyen fails to teach combining a second output of the variable gain amplifier circuit and the output of the g_m switch to provide a corrected signal, but has asserted that Fig. 31b of Nguyen discloses similar connections. However, as the Examiner has stated, what is shown in Fig. 31b of Nguyen is the connection of a differential pair amplifier and a *linearization circuit*, not a VGA circuit and a *g_m switch*. The linearization circuit in Nguyen and the g_m stage in Briskin have completely different functions. There is no motivation for a skilled artisan to replace the linearization circuit in Fig. 31b of Nguyen with the g_m stage in Briskin.

Accordingly, Applicant respectfully submits that it is improper for the Examiner to combine Nguyen and Briskin.

Even if a skilled artisan were to combine the two references, as the Examiner has suggested, the combination would not result in the invention of claim 1. As discussed above, neither Nguyen nor Briskin teaches or suggests correcting an asymmetric signal. Further, the g_m switch in claim 1 provides an output having only a first polarity. Neither of the references discloses or suggests this feature.

Accordingly, Applicant respectfully submits that claims 1-14 are patentable over the combination of Nguyen and Briskin.

Like claims 1-14, claims 15-59 recite, among other things, correcting an asymmetric signal. Accordingly, claims 15-59 are patentable over the combination of Nguyen and Briskin at least for the same reasons as those for claims 1-14.

2. Goh Fails to Remedy the Deficiencies of Nguyen and Briskin

Goh provides a method for compensating **digital** samples of an asymmetric read signal.

A compensator is shown in Fig. 6 of Goh:

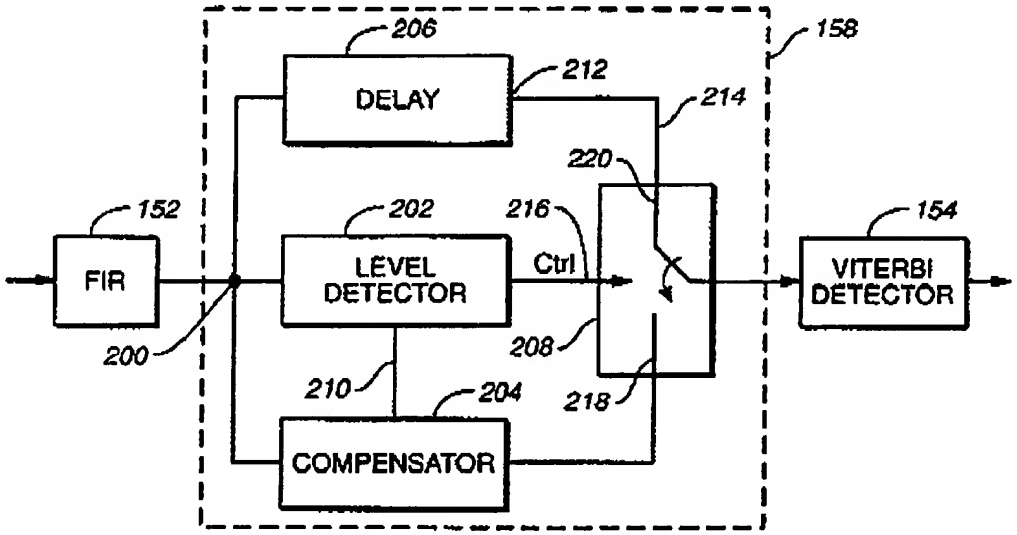

FIG._6

Goh states (emphasis added):

> One embodiment of the asymmetry correction block includes an input 200, a level detector 202, a compensator 204, and an output 208. The input receives **a digital sample of the asymmetric read signal** V(t) and provides the digital sample to level detector 202 and compensator 204. Level detector 202 determines whether the digital sample requires compensation. If it is determined that the digital sample requires compensation, compensator 204 generates a compensated sample. The output 208 is configured to selectively output either the digital sample or the compensated sample. In one embodiment of the invention, the asymmetry correction block 158 further includes a delay circuit 206. Delay

> circuit 206 receives the digital sample from input 200 and delays providing it to output 208 to ensure proper synchronization with compensator 204. (Goh, col. 8, line 62 to col. 9, line 10).

Although Goh is related to correcting an asymmetric signal, what is corrected in Goh is the *digital sample* of the asymmetric signal. Goh does not indicate any need for the g_m stage in Briskin, or how to integrate the g_m stage in Briskin into the circuit shown in Fig. 6. Accordingly, Applicant submits that the Examiner's combination of Goh, Nguyen and Briskin is improper, and claims 29-31, 33, 55-57 and 59 are patentable for this additional reason as well.

Request for Allowance

It is believed that this Amendment places the application in condition for allowance, and early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number listed below.

Atty. Docket No. MP0392
PATENT APPLICATION

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The Office is hereby authorized to charge any fees, or credit any overpayments, to

Deposit Account No. **11-0600.**

Respectfully submitted,
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Dated: June 22, 2006

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